Karlsruhe Institute of Technology

Low Power Design

Victor M. van Santen & Volker Wenzel on behalf of Prof. Henkel
Sommersemester 2016

CES – Chair for Embedded Systems

.. with Hussam Amrouch

Lecture Slides

Overview Low Power Design Lecture

- Introduction and Energy/Power Sources (1)
- Energy/Power Sources(2): Solar Energy Harvesting
- Battery Modeling – Part 1
- Battery Modeling – Part 2
- Hardware power optimization and estimation – Part 1
- Hardware power optimization and estimation – Part 2
- Hardware power optimization and estimation – Part 3
- Low Power Software and Compiler
- Thermal Management – Part 1
- Thermal Management – Part 2
- Aging mechanisms in integrated circuits
- Lab Meeting

Lab Meeting

- Lab Meeting
  July, 21th 2016 at 9:45

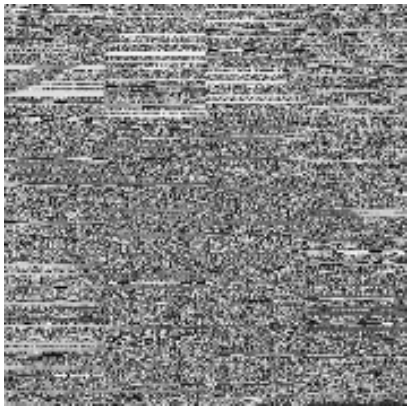
- Technologiefabrik
  Haid-und-Neu-Straße 7
  2nd floor

- Relevant for the oral examination

Outline

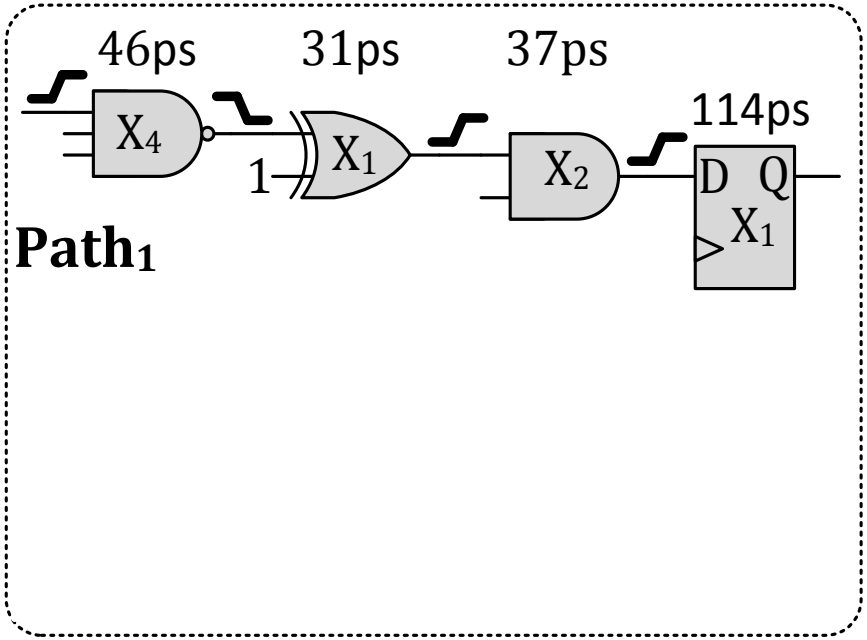
- What is Aging?
- Aging in Transistors
- Aging Models & Stimuli
- Aging in Metal Interconnects
- Impact of Applications on Aging
- Safety Margin
- Mitigation Techniques
- Conclusion

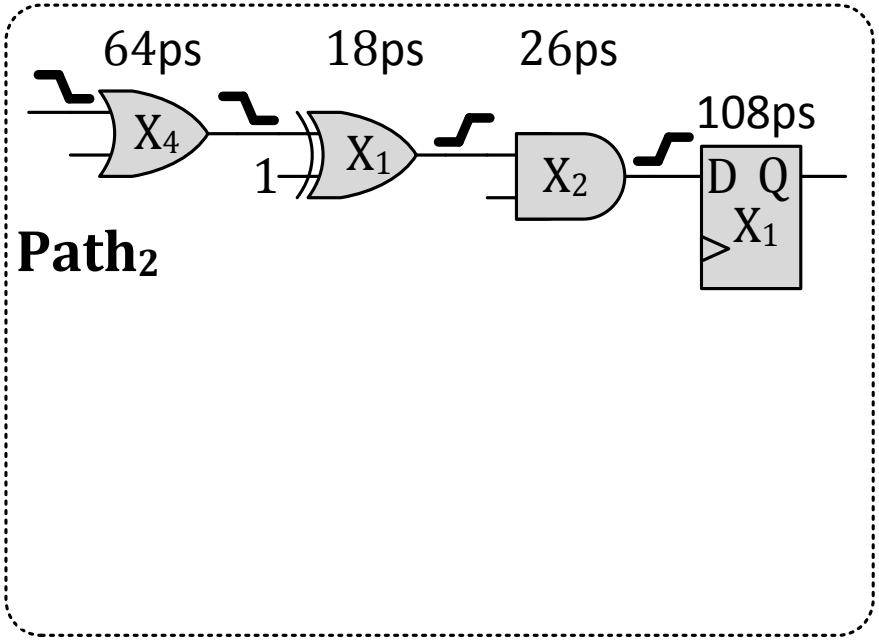
What is Aging?

Original Design	Reliability-Unaware Design	
Violated Paths: 0	Violated Paths: 45	Violated Paths: 271
		
Original Image	**Year 1** (**Balanced** Aging)	**Year 1** (**Worst** Aging)
Peak Signal to Noise Ratio = 38dB	PSNR = 18dB	PSNR = 9dB

Src. Amrouch, et al. “Reliability-Aware Design to Suppress Aging”, DAC’16

Aging increases Path Delay





Before Aging: Total Delay = 114ps

Before Aging: Total Delay = 108ps

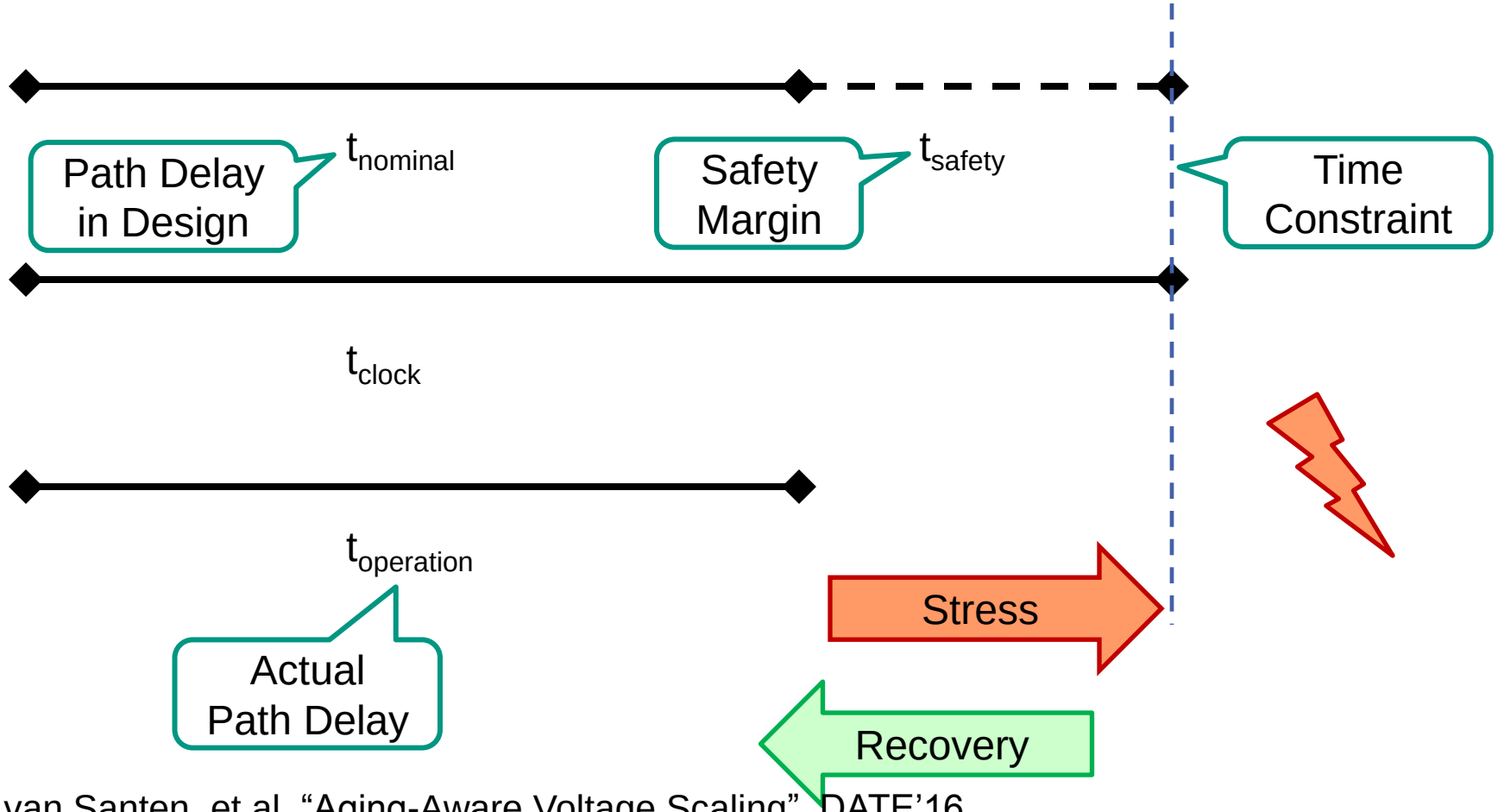
After Aging: Total Delay = 119ps

After Aging: Total Delay = 121ps

Src. Amrouch, et al. “Reliability-Aware Design to Suppress Aging”, DAC’16

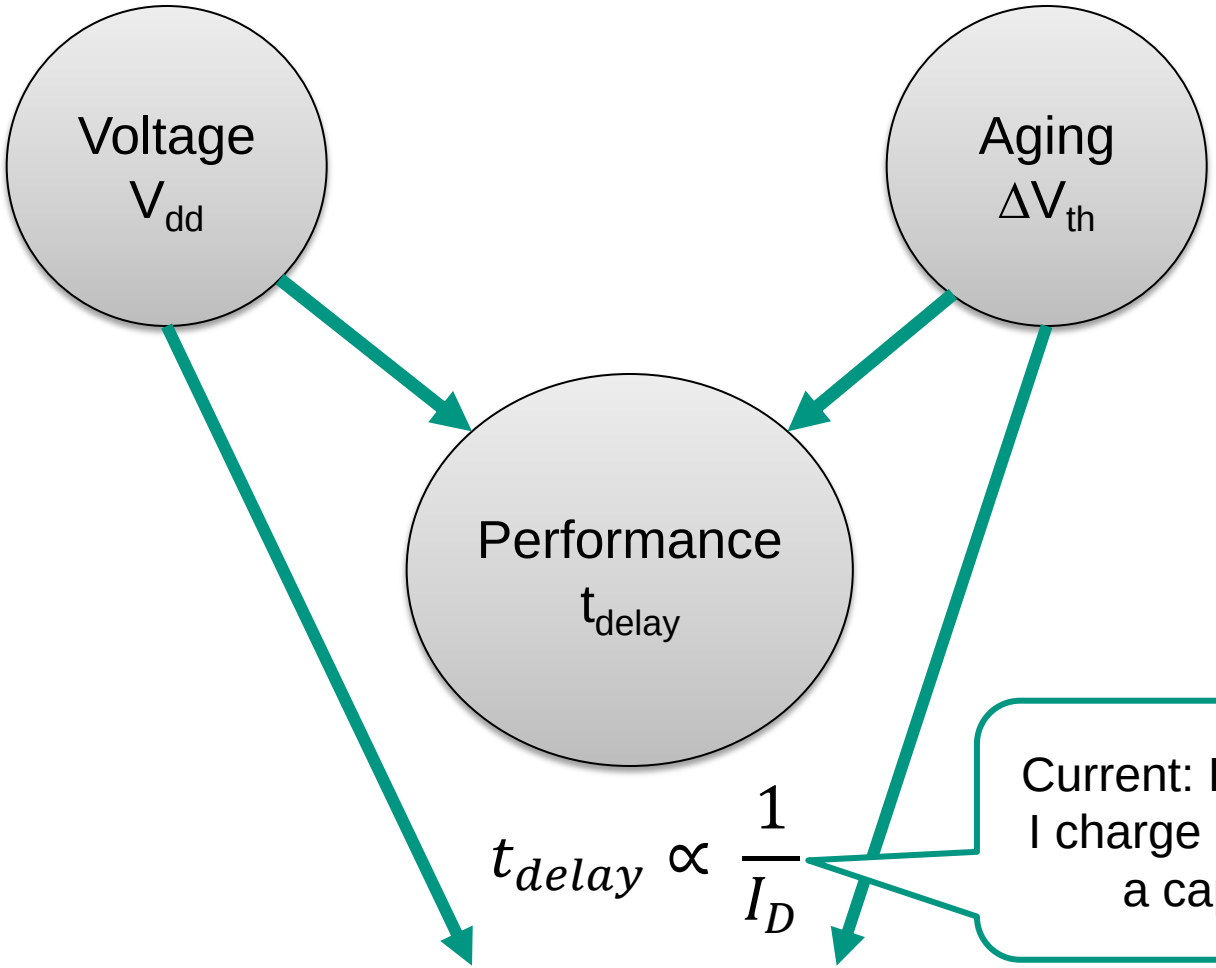
Timing Violations due to Aging

- Aging degrades reliability over time (e.g. years)



Src. van Santen, et al. “Aging-Aware Voltage Scaling”, DATE’16

Impact of Aging on Path Delay

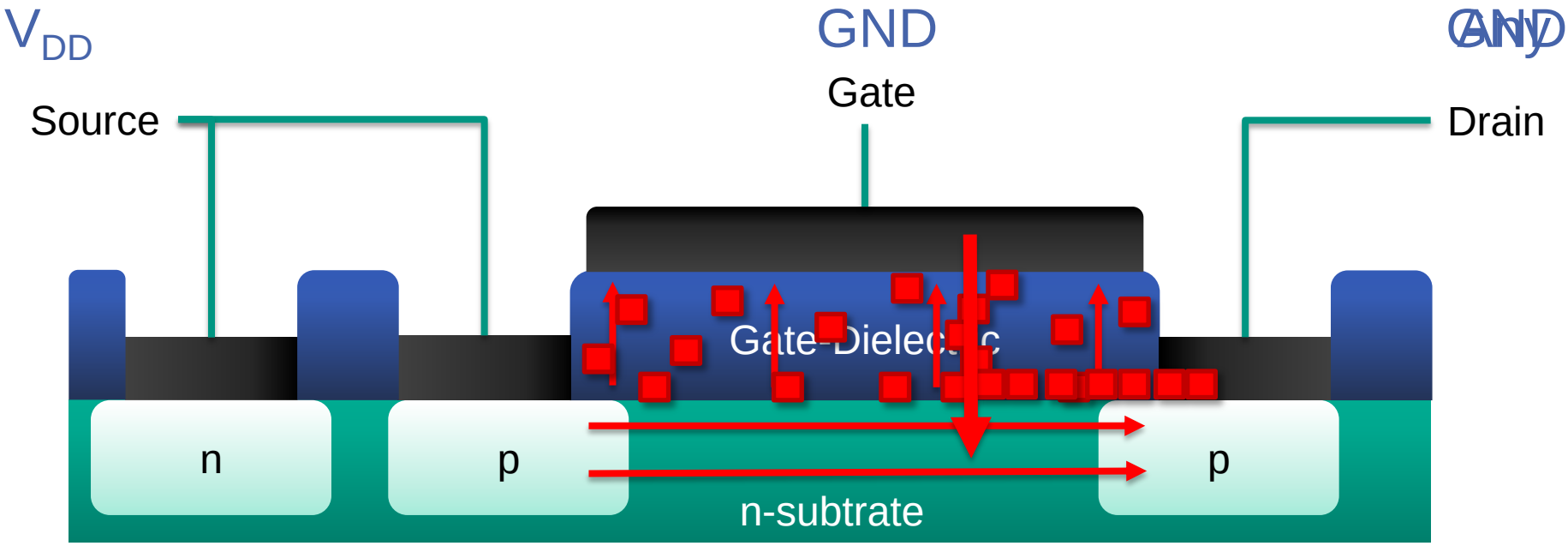


Aging Phenomena

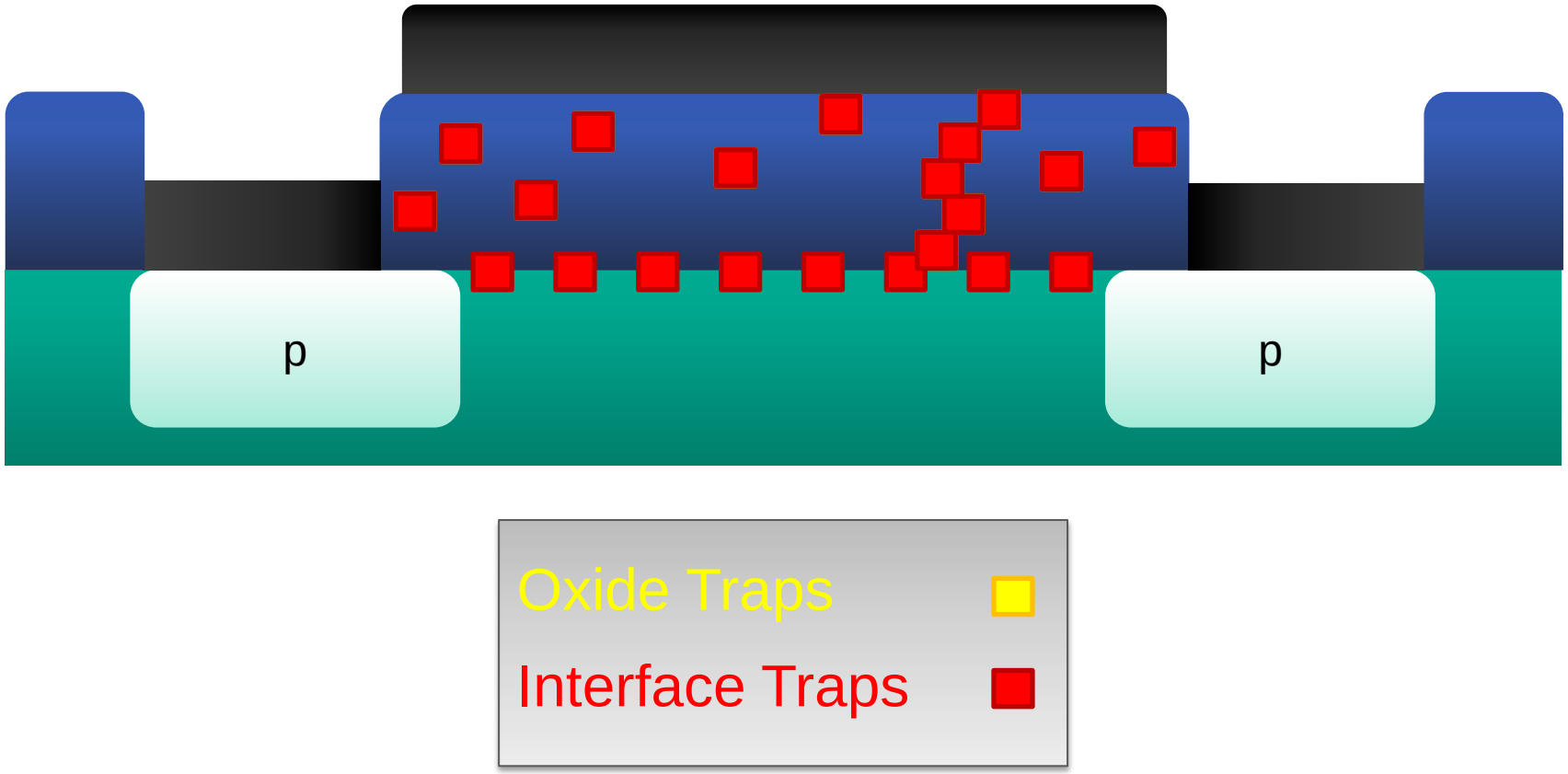
- Bias Temperature Instability (BTI)
  - Electric Field over Gate Dielectric creates defects
- Hot Carrier Induced Degradation (HCID)
  - Fast electrons knock out atoms and create defects
- Time Dependent Dielectric Breakdown (TDDB)
  - Defects in Gate Dielectric form conductive Path and high current flow melts the transistor
- Electro Migration (EM)
  - Fast electrons knock out atoms in interconnects

Aging in Transistors

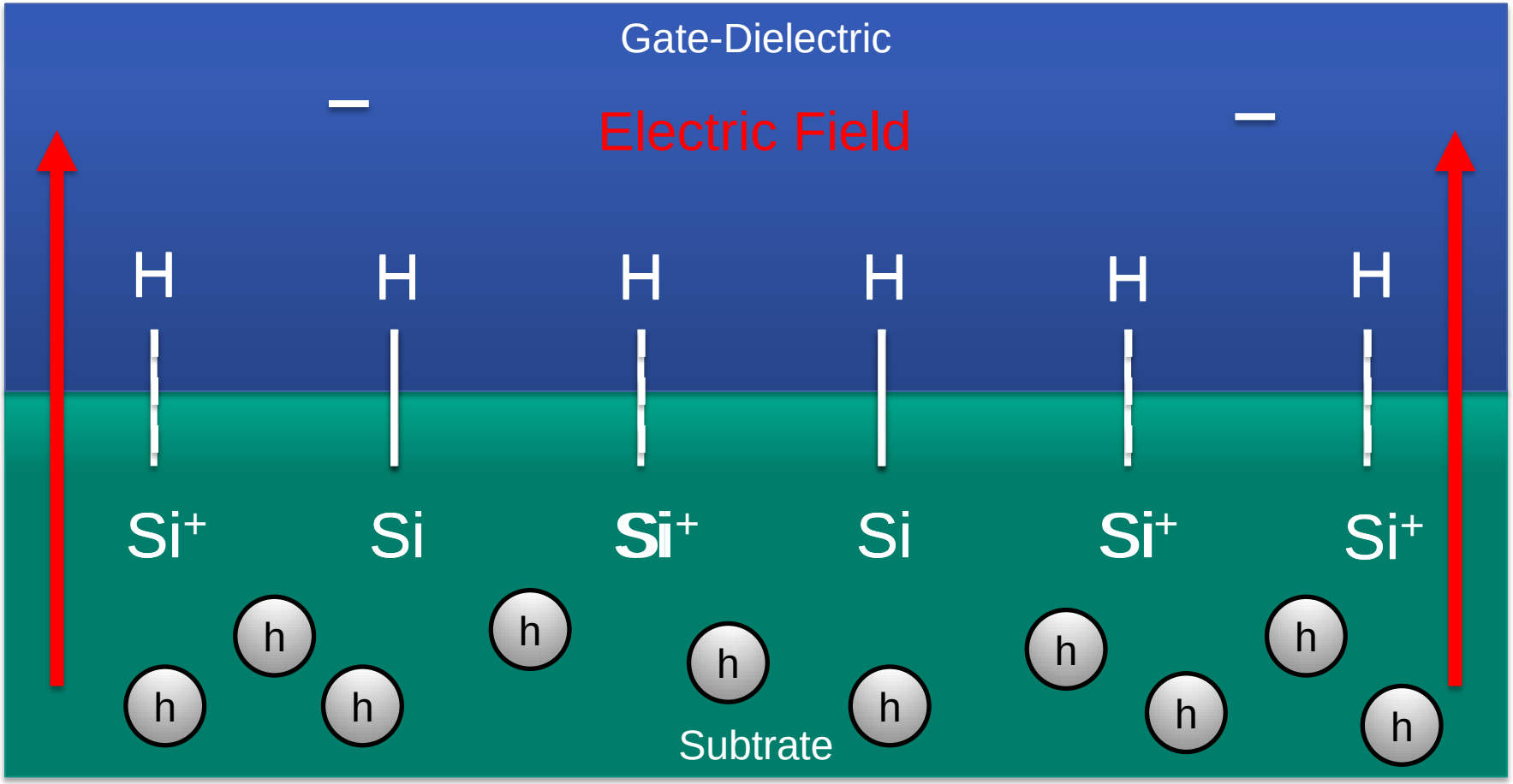
- Three Key Aging Phenomena in Transistors
  - Bias Temperature Instability (BTI)
  - Time Dependent Dielectric Breakdown (TDDB)
  - Hot Carrier Induced Degradation (HCID)



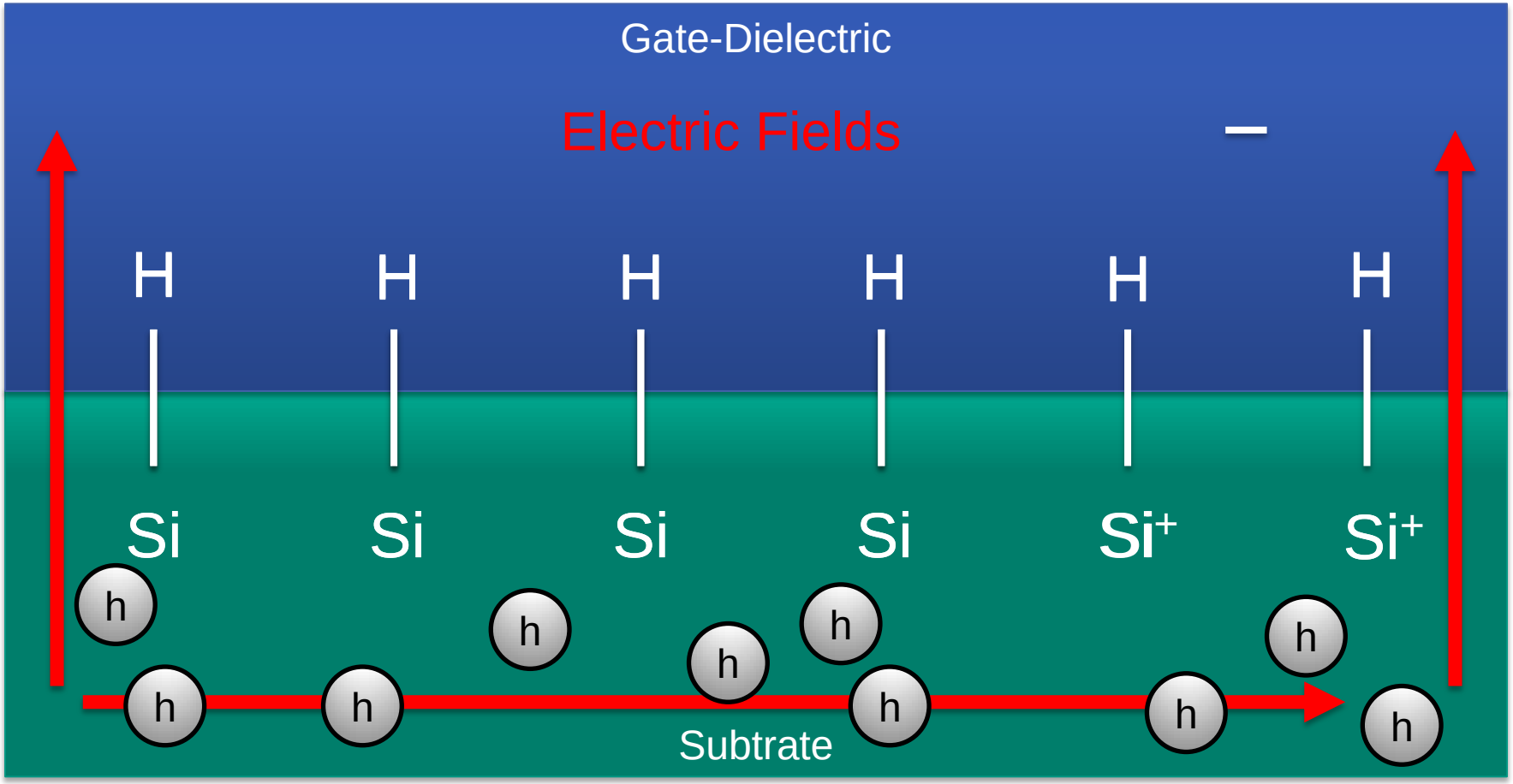
Aging in Transistors - Two Types of Defects



Interface Traps due BTI

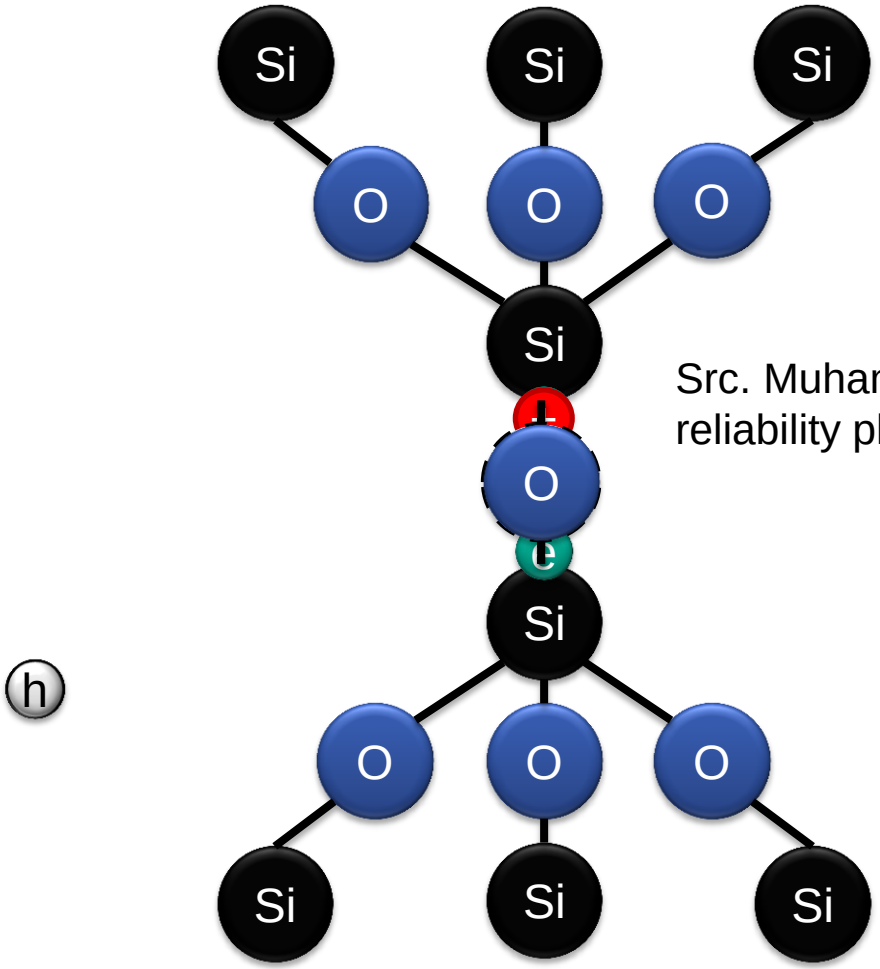


Interface Traps due Hot Carriers



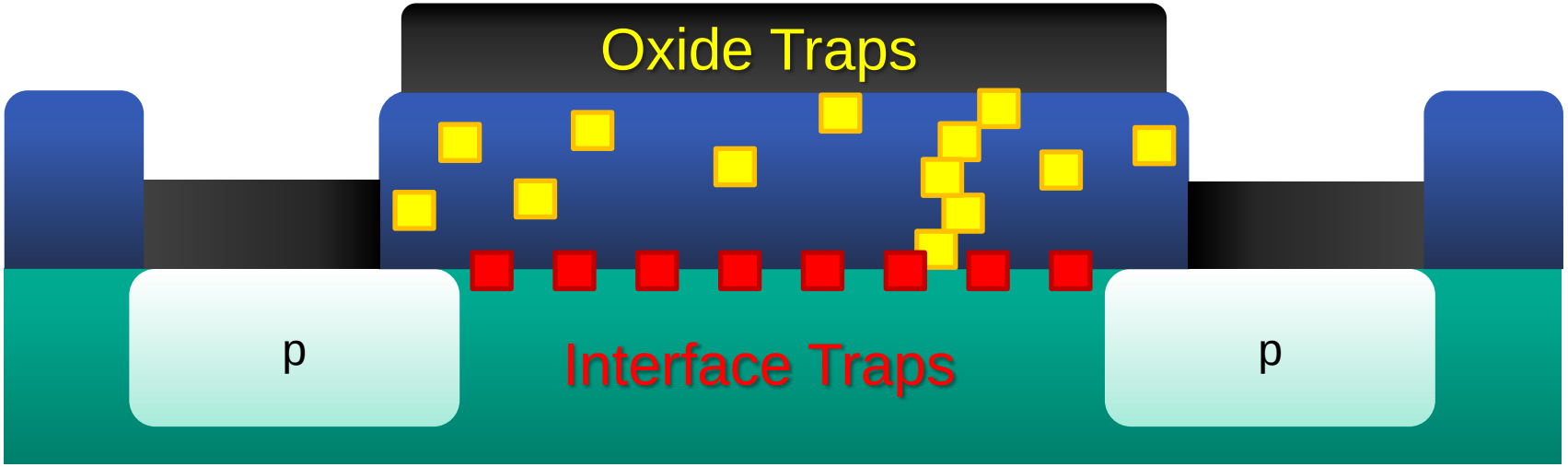
Oxide Traps

- Oxide Traps are Oxide Vacancies



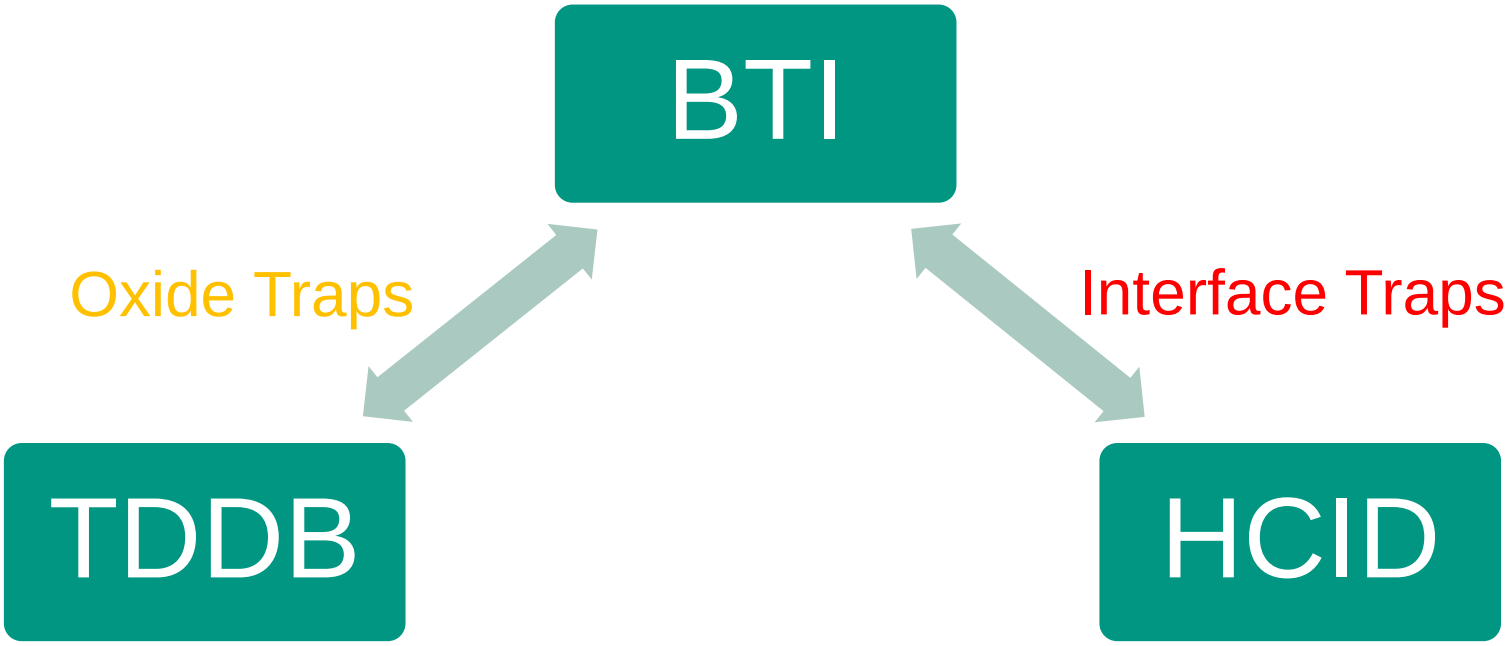
Src. Muhammad A. Alam. Ece 695a reliability physics of nanotransistors, 2013

Background – Summary



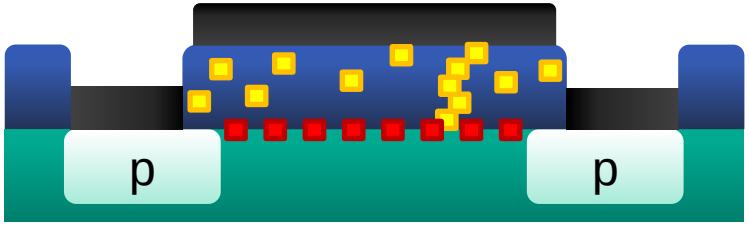
- Oxide Traps
  - Located deep in Gate-Dielectric
  - Oxide vacancies
  - Positive Charge
  - Pre-existing due Manufacturing & Generation during Operation
- Interface Traps
  - Located at interface between dielectric and subtrate
  - Broken Si-H bonds
  - Positive Charge
  - Generated during Operation

Background – Interactions Aging Phenomena



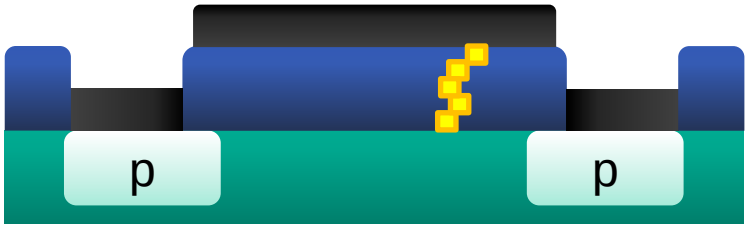
Transistor Aging Models

- BTI Reaction Diffusion Model
  - Interface & Oxide Traps
  - Stress by Electric Field
  - Thermal Activation



- HCID Reaction Diffusion Model
  - Interface Traps
  - Stress by Hot Carriers
  - Kinetic Activation

- TDDB Stochastic Model
  - Only Hard Breakdown
  - Probabilistic Model based on Weibull Distribution



Existing Aging Models

Fitted Analytical Equations

Modeling physical processes

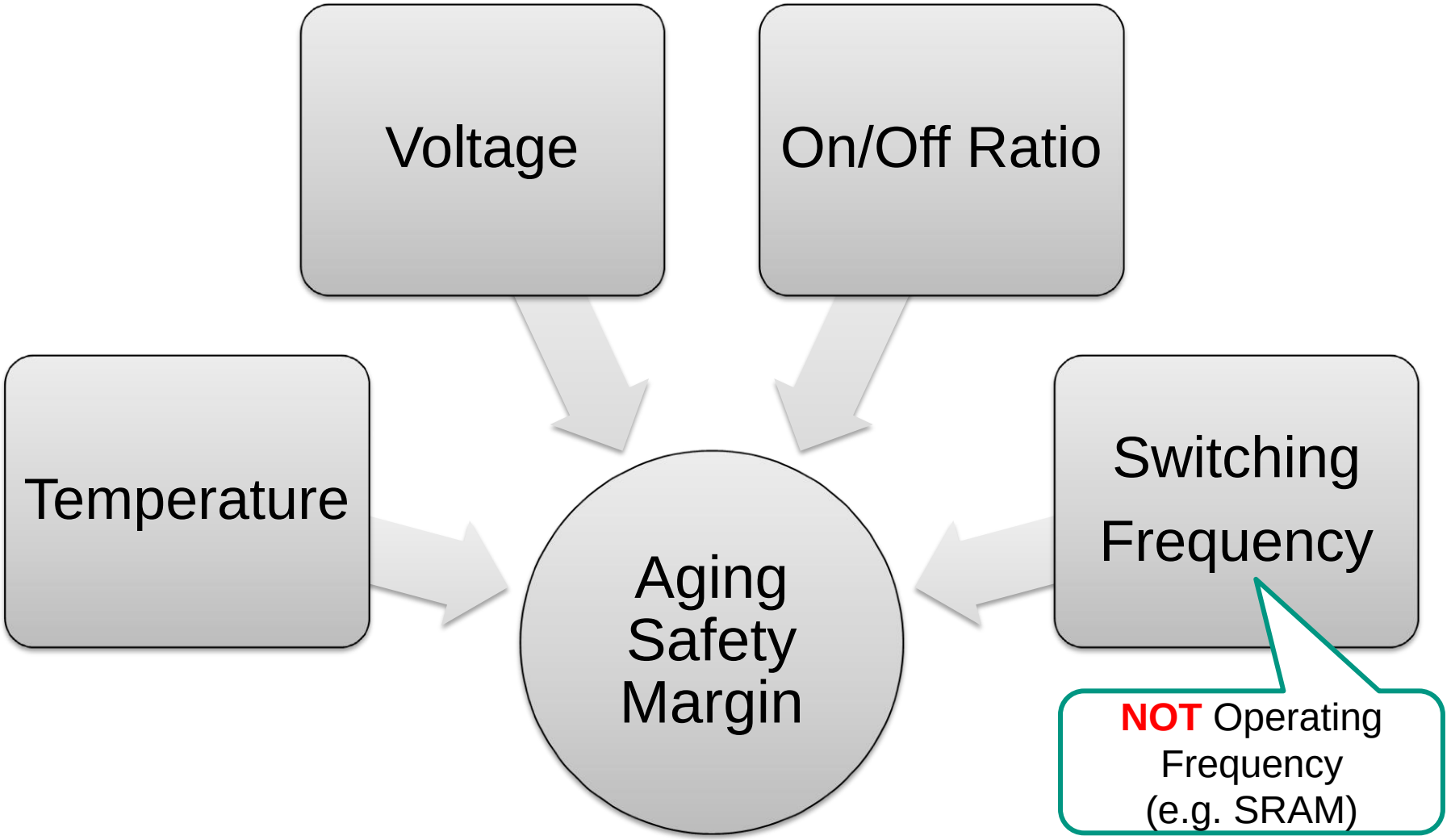
	Empirical Model	Physical Model
Long-Term Aging	✓	✓
Short-Term Aging	✗	✓
Time per Transistor	1 millisecond	7 Minutes
Feasible for Circuits	✓	✗
Calibrated with	Chip Failures	Transistor Measurements

→ High Uncertainty

→ Low Uncertainty

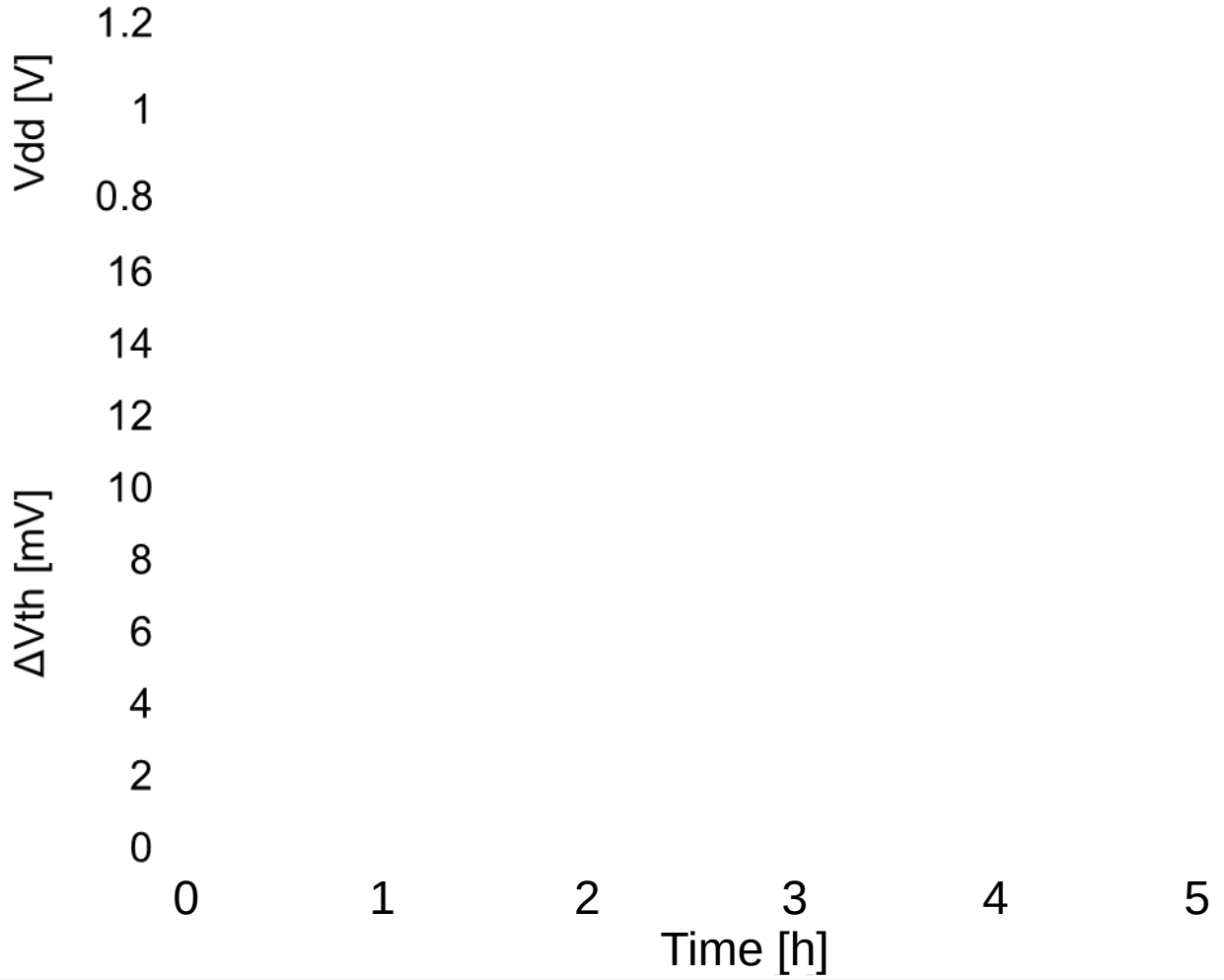
Src. van Santen, et al. “Designing Guardbands for Instantaneous Aging Effects”, DAC’16

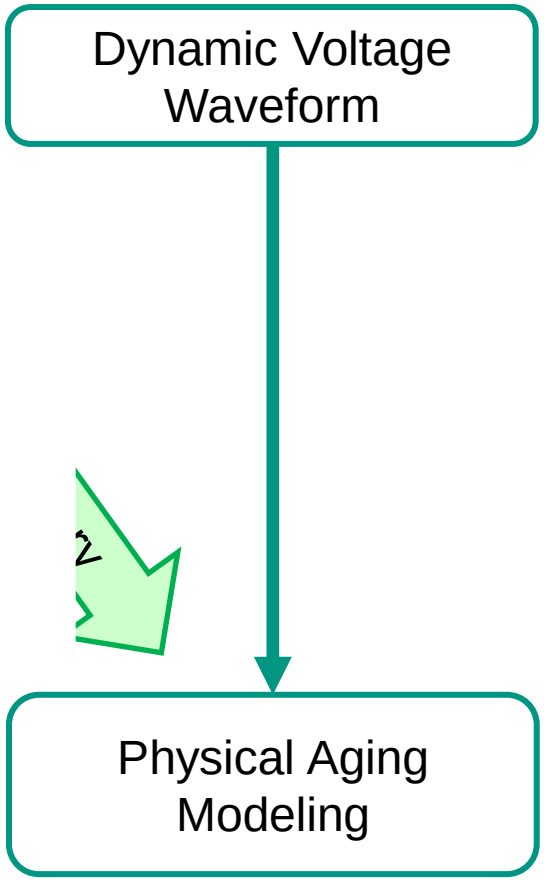
Aging Stimuli



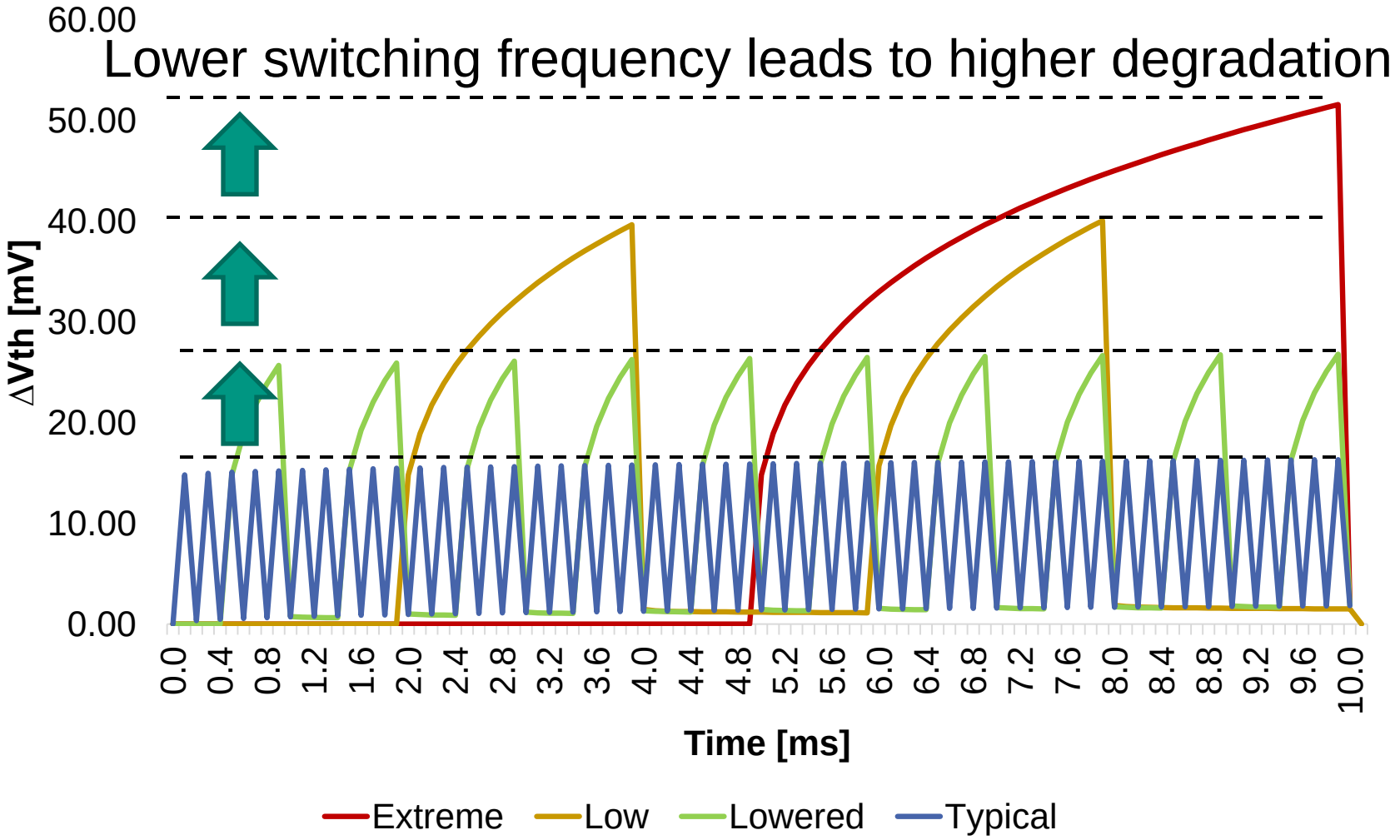
BTI / HCID feature recovery

- Aging is stimulated by V_{dd}





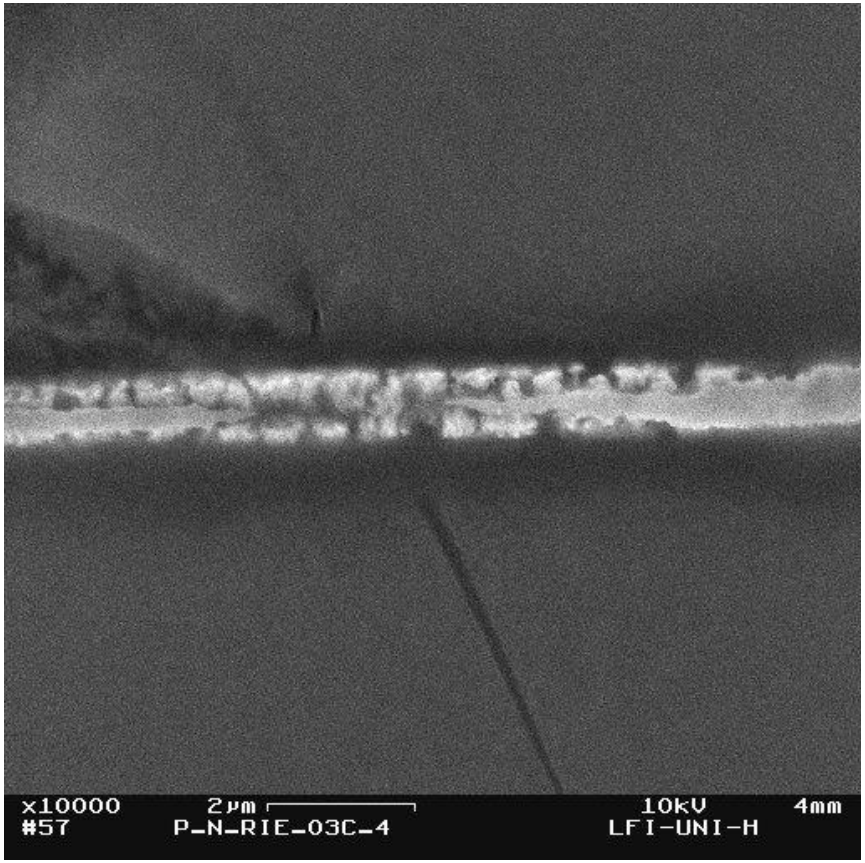
BTI is Frequency Dependent



Src. van Santen, et al. “Designing Guardbands for Instantaneous Aging Effects”, DAC’16

Aging in Metal Interconnects

- Electromigration
  - Degrades wires
    - Power distribution network
    - Data connections
  - Carriers take metal atoms and move them
  - Stimuli
    - Current density
    - Temperature



src: http://en.wikipedia.org/wiki/Electromigration

Impact of Application on Aging

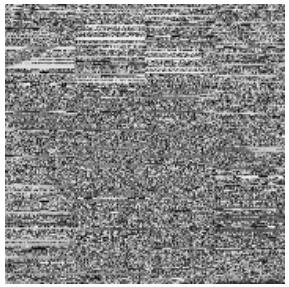
Before Aging

Towards Where Aging Effects Originate

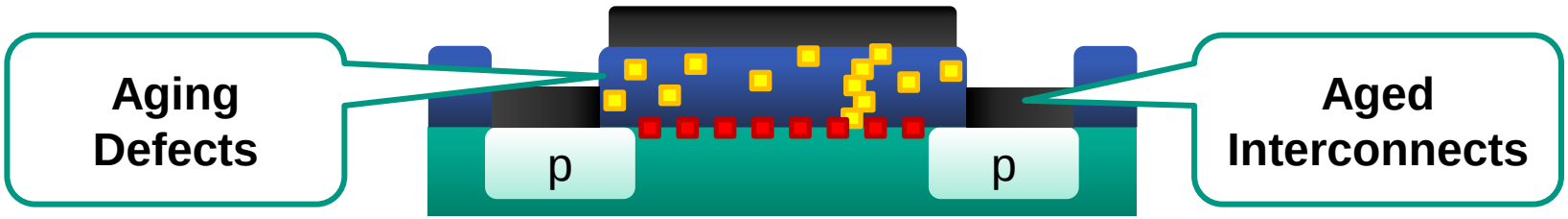
- System Level
- Circuit Level
- Gate Level
- Transistor Level
- Physical Level

Towards Where Aging Effects Manifest Themselves

Application

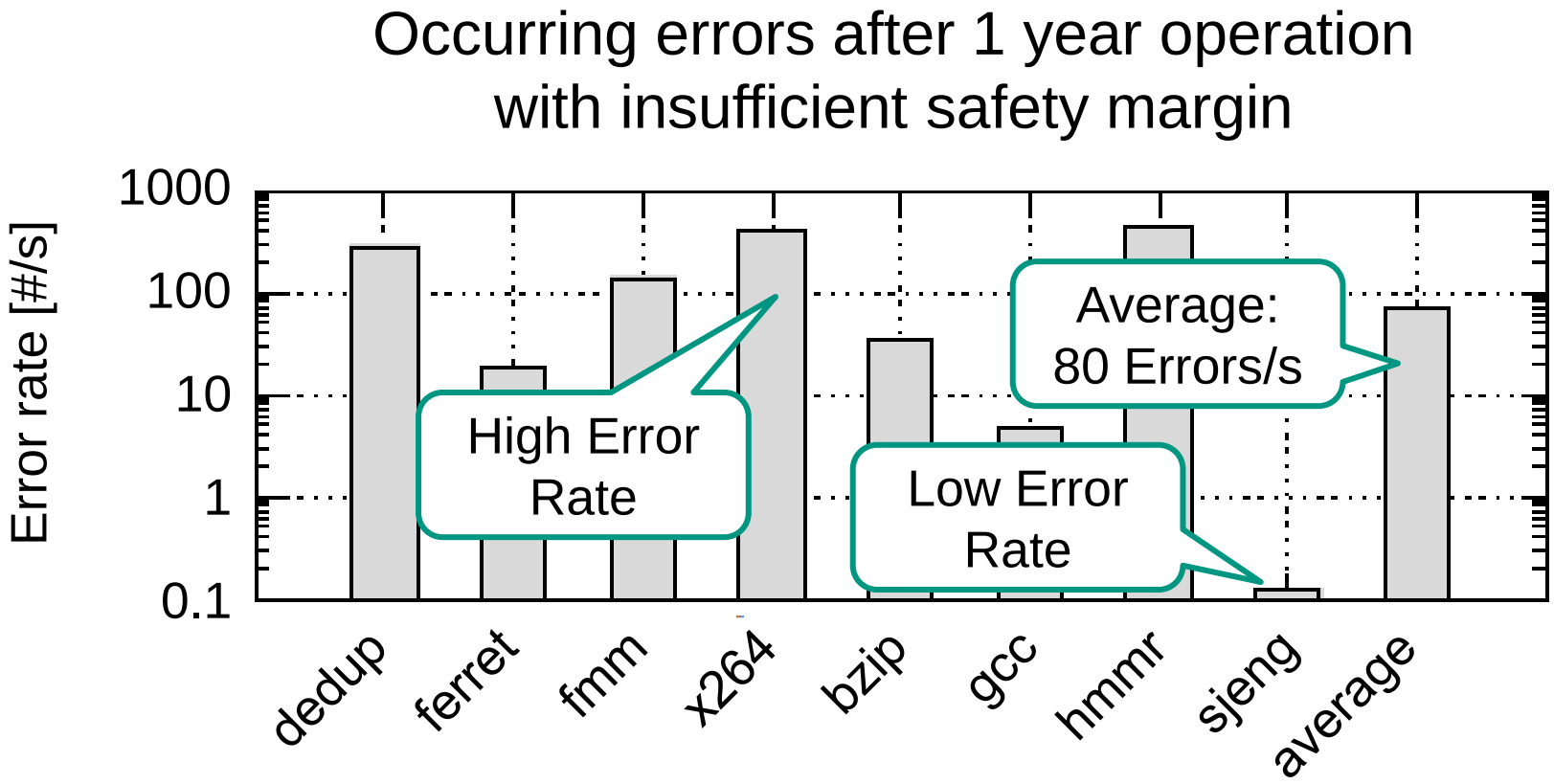


After Aging



Src. Amrouch, et al. “Reliability-Aware Design to Suppress Aging”, DAC’16

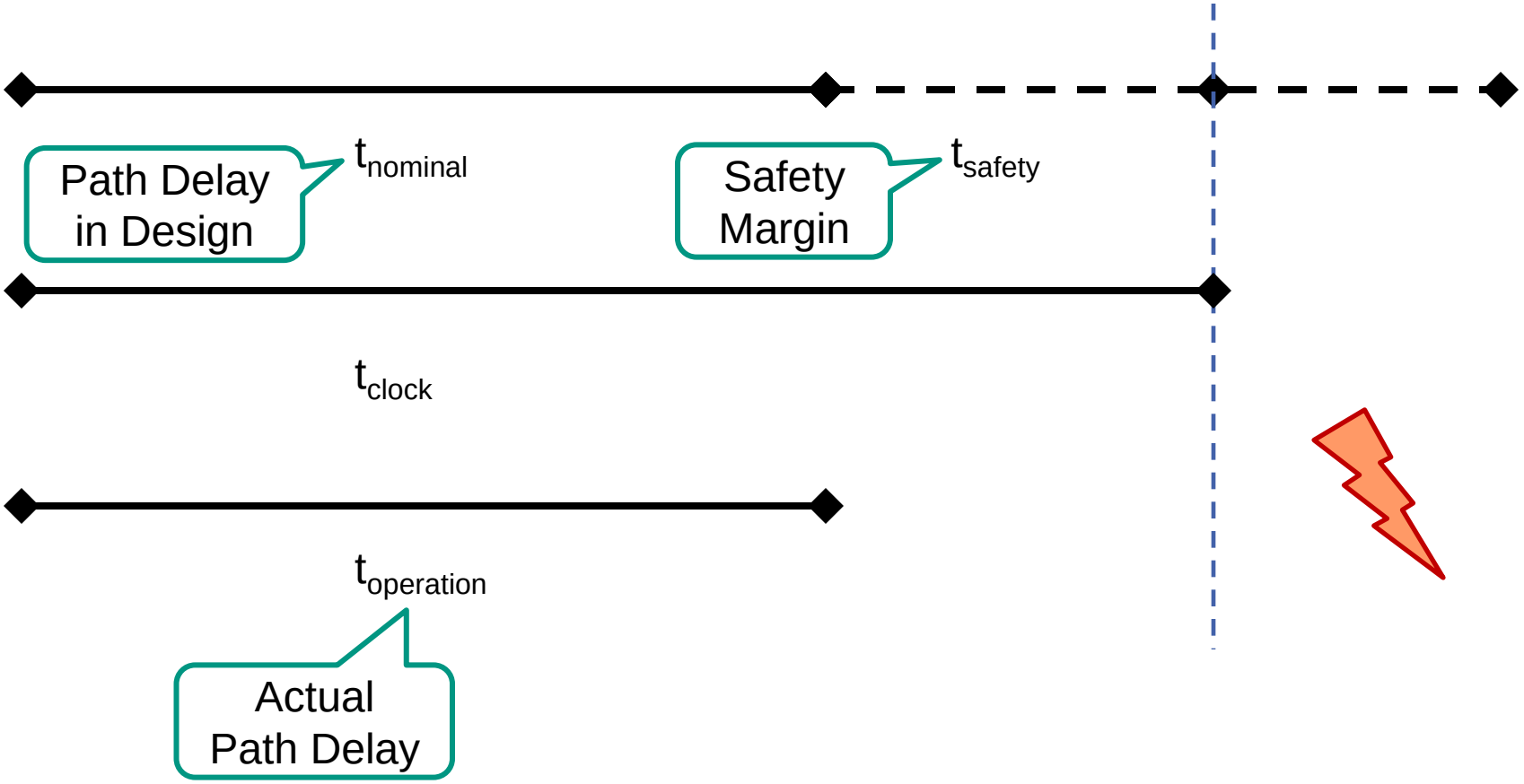
Errors depend upon Application



Src. van Santen, et al. “Aging-Aware Voltage Scaling”, DATE’16

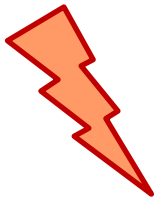
Employ Safety Margins

- Increase safety margin to tolerate degradation



Impact of Selecting Safety Margin

- Increased safety margins manifests themselves as
  - Higher performance loss
  - Higher area overhead
  - Higher power overhead
- Too low safety margins
  - Errors



- Estimate actually required safety margins
  - Efficient & safe designs

Mitigation Techniques

- Reduce Aging Stimuli
  - Lower Temperature – Thermal Management
  - Lower On-/Off-Ratio – Duty Cycle Balancing
  - Lower Voltage – Dynamic Frequency Voltage Scaling (DVFS)
  - Higher switching frequency – Periodic Inversion
- Less stimuli → Less aging
  - Less safety margins → More efficient system
- Hardware/Software
  - Modify application/compiler
  - Modify hardware architecture
  - Modify environment (cooling, etc.)

Conclusion

- Aging degrades circuits (performance & power)
  - Depends upon stimuli from applications
  - BTI, HCID, TDDB & EM
- Over-design to tolerate degradations
  - Safety margin
  - As small as possible, yet still safe
- Mitigate aging
  - Reduce aging stimuli
  - Minimize safety margins

Literature

- Hussam Amrouch, Behnam Khaleghi, Andreas Gerstlauer, Jörg Henkel, “Reliability-Aware Design to Suppress Aging in ACM/EDAC/IEEE 53rd Design Automation Conference (DAC), 2016.
- Victor M. van Santen, Hussam Amrouch, Javier Martin-Martinez, Montserrat Nafria, Jörg Henkel, “Designing Guardbands for Instantaneous Aging Effects” in ACM/EDAC/IEEE 53rd Design Automation Conference (DAC), 2016.
- Victor M. van Santen, Hussam Amrouch, Narendra Parihar, Souvik Mahapatra, Jörg Henkel “Aging-Aware Voltage Scaling” in IEEE/ACM 19th Design, Automation and Test in Europe Conference (DATE), 2016.
- Hussam Amrouch, Victor M. van Santen, Thomas Ebi, Volker Wenzel, Jörg Henkel “Towards Interdependencies of Aging Mechanisms” in IEEE/ACM 33rd International Conference on Computer-Aided Design (ICCAD), 2014.

http://ces.itec.kit.edu/dependable-hardware.php

Literature

- Nanohub Lecture by Muhammed Alam
  https://nanohub.org/resources/16560#series
  BTI, HCID, TDDB, Soft Errors → Lecture (Video + Slides)
- S. Mahapatra, N. Goel, S. Desai, S. Gupta, B. Jose, S. Mukhopadhyay et al., “A Comparative Study of Different Physics-Based NBTI Models,” T-ED, 2013
- X. Li, J. Qin, and J. Bernstein, “Compact Modeling of MOSFET Wearout Mechanisms for Circuit-Reliability Simulation,” TDMR, 2008
- Bias Temperature Instability for Devices and Circuits, Tibor Grasser, Springer 2014 → Book

Bachelor/Master Thesis

- Interested in Bachelor/Master Thesis?
  (Computer Science, Electric Engineering, Physics, Mathematics)
  - Reliability Modeling
    - Aging
    - Soft Errors
    - Manufacturing Variability
  - Circuit Simulations & Optimization
    - Simple Circuits (Adder, Multiplier)
    - Micro-Processors
  - CUDA Programming
    - Parallelize aging models
    - Achieve high speed-ups through parallelization
- Contact us:

http://ces.itec.kit.edu/~amrouch/
http://ces.itec.kit.edu/~vansanten/